方案

单位：元

产品名称	型号	数量	单价	总价	生产厂家	备注
FPGA 多媒体开发平台	DE2-70	25	3290	82250	台湾友晶	数量根据学校要求
FPGA 开发平台	DE4	2	29950	59900	台湾友晶	
4.3 英寸数字 LCD 触碰面板套件	LTM	5	1700	3400	台湾友晶	
500 万像素数字相机模块卡	D5M	5	850	4250	台湾友晶	
高速 数位-模拟/模拟-数位 模组卡-HSMC	ADA-HSMC	2	2190	4380	台湾友晶	
合计	人民币：154180 元					

注：Altera 共建联合实验室优惠条件：

1. DE2-70 按照学术价格 3290 元/套，实际数量共 25 套（硬件赠送套数 5 套）。

2. 软件免费赠送：40 万美金的软件 30 年授权。

下列的表格共参考，详细细节由 Altera 公司的徐总和贵校负责人详谈。

Altera 共建联合实验室预算合计：154180 元

Oriental Institute of Technology and Altera International Limited

Joint EDA/SOPC Lab

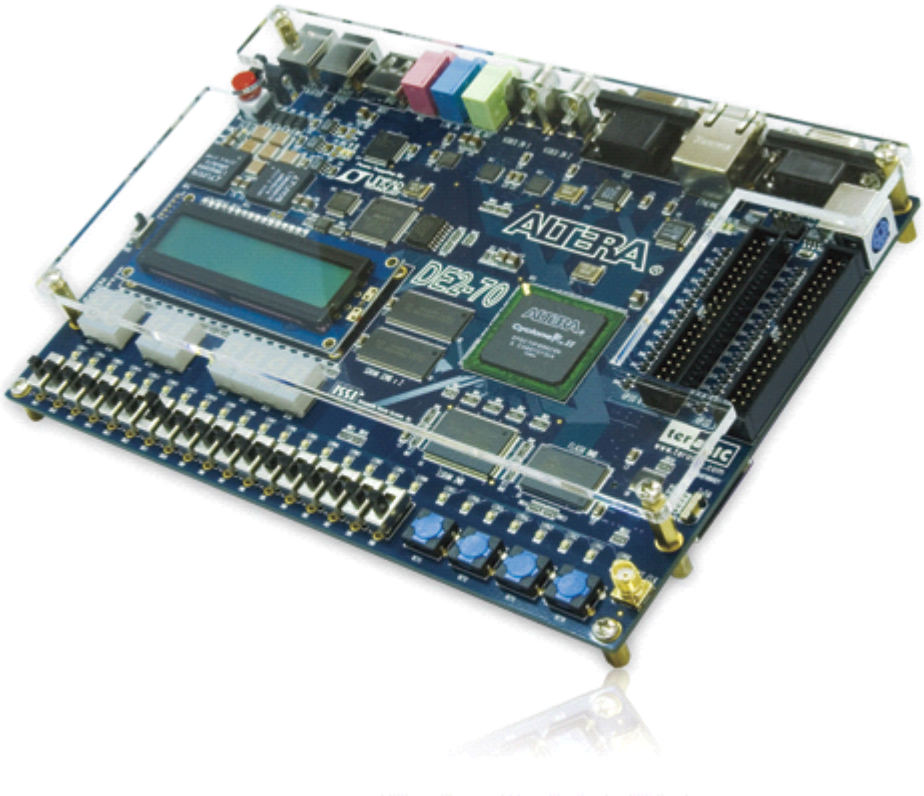
The objectives of the Joint EDA/SOPC Lab are:

1) Develop and support EDA/SOPC technology education in Oriental Institute of Technology
2) Support talent development of EDA/SOPC technology expertise in Oriental Institute of Technology

In setting up this Joint EDA/SOPC Lab, Altera agrees to donate the following development tools, software and IP Cores, which are exclusively governed by the applicable standard license agreements:

Category	Description	Quantity
Design Software	Quartus II (FLOATPC)	50
	Nios II (SOPC Builder Inculded)	50
Development Tools	DSP Builder	50
	C2H Compiler	50
MegaCore	Video and Image Processing Suite (Color Space Converter Included)	50
Memory Controller MegaCore	DDR SDRAM Controller	50
	DDR SDRAM High Performance Controller	50
	DDR2 SDRAM Controller	50
	DDR SDRAM High Performance Controller	50
	QDRII SRAM Controller	50
	RLDRAM II Controller	50
Interfaces MegaCore	32-bit PCI Bus Master/ Target interface	30
	SerialLate II	10
	Triple Speed Ethernet	10
	Video Interface - ASI	10
	Video Interface - SDI	10
Signal Processing MegaCore	FIR Compiler	30
	NCO Compiler	10
	Reed-Solomon Encoder	10
	Reed-Solomon Decoder	10
	Viterbi High Speed Decoder	10
	Viterbi Low-Speed Decoder	10
	FFT/IFFT	30
	CIC	10

DE2-70 多媒体开发平台



Altera DE2-70 最新多媒体开发平台配备了数量高达 70,000 个逻辑单元的 Altera Cyclone® II 2C70 和更大容量的内存组件，并完全承袭了 Altera DE2 多媒体平台丰富的多媒体、储存及网络等应用接口的优点。此开发平台提供多样的产品功能，不仅适用于大专院校实验室的教学研究与专题制作，也适合工业界做为开发复杂数字系统的工具，Altera 更为此最新多媒体开发平台提供现成的实验课教材和各种说明范例。

产品规格：

Altera DE2-70 最新多媒体开发平台提供使用者丰富的产品功能，在广泛的电路设计运用上，从简易的电路设计，到多样化的多媒体项目，使用者都能轻易完成。

FPGA

- Cyclone II 2C70 FPGA
  - 70,000 LEs (逻辑单元)

内存

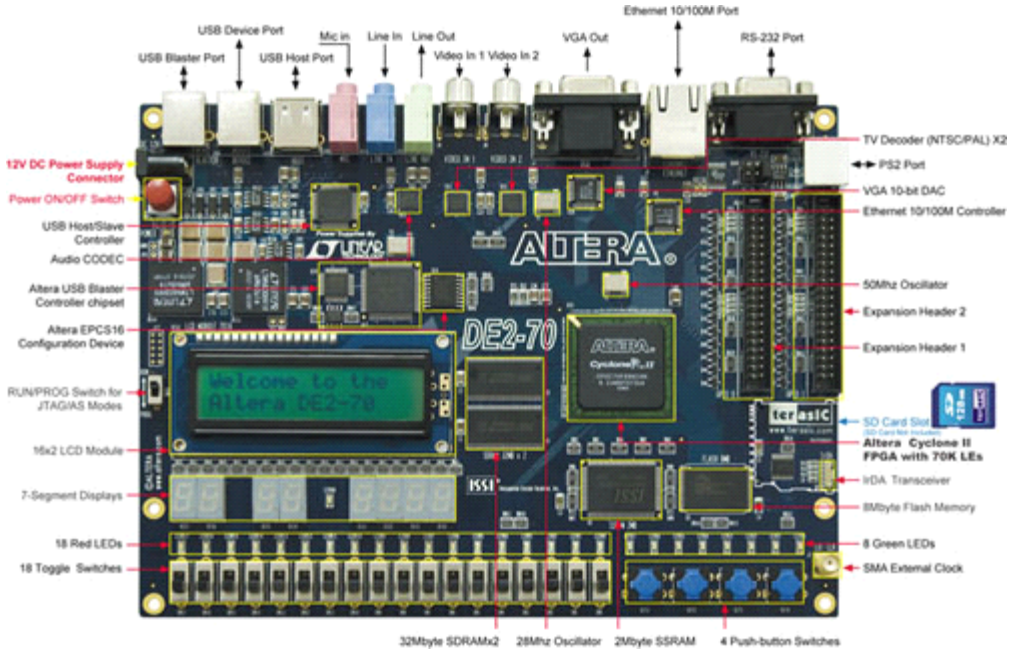
- SDRAM
  - 2个 32-Mbyte SDRAM
- SRAM
  - 1个 2-Mbyte SRAM
- Flash memory
  - 8-Mbyte Flash 内存
- SD card socket
  - 支持 SPI 以及 SD 1-bit 两种 SD Card 读取模式

界面

- 内建 USB Blaster 电路
  - 内建 USB Blaster 使用于 FPAG 程序下载或控制
  - 支持 JTAG 与 AS 模式

- Altera 序列配置器
  - Altera EPCS16 序列 EEPROM
- 按钮与滑动开关
  - 4个按钮
- 滑动开关
  - 18 个滑动开关
- 人机界面
  - 9 个绿色 LEDs
  - 18 个红色 LEDs
  - 8 个七段显示器
  - 16 x 2 LCD 模块
- 传输接口
  - 10/100MHz 以太网络控制器和接头
  - IrDA 收发模块
  - 1个 SMA 接头
- USB 界面
  - USB 主/从控制器
  - Type A 和 Type B 的接头
- Clock 输入
  - 50MHz 振荡器
  - 28.63MHz 振荡器
- TV 输入
  - 2 个 TV 讯号译码器
  - 2 个 TV 输入讯号连接头
- VGA 输出
  - 3个10-bit 高速 DAC (数字模拟转换)
- Audio 输入与输出
  - 24-bit CD 质量的输入、输出与麦克风输入接头
- 序列接头
  - 一组 RS-232 讯号接头
  - 一组 PS/2讯号接头
- 两组40个接脚扩充槽
  - 72 个 I/O 接脚以及8个电源与接地接脚

组件配置：



- Size：153*203 mm

设计资源：

档案下载

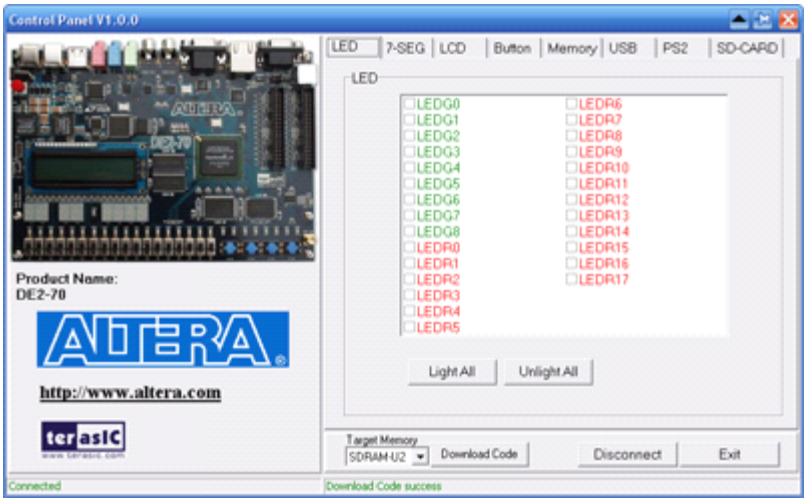
DE2-70 CD-ROM 下载连结
http://www.terasic.com/downloads/cd-rom/de2-70/

Document

标题	日期	下载
DE2-70 User manual	2009-11-06	

DE2-70 示范

- DE2-70 控制面板工具程序
- DE2-70 影像工具程序
- 电视盒
- 电视盒 Picture in Picture 子母画面
- USB Paintbrush 展示
- USB 装置功能展示
- 卡拉 OK 机 功能展示
- 乙太网 络封包传递功能展示
- SD 卡音 乐播放程序功能产示
- 音乐合成器功能产示
- 音乐录制及播放功能



DE2-70 Contorl Panel

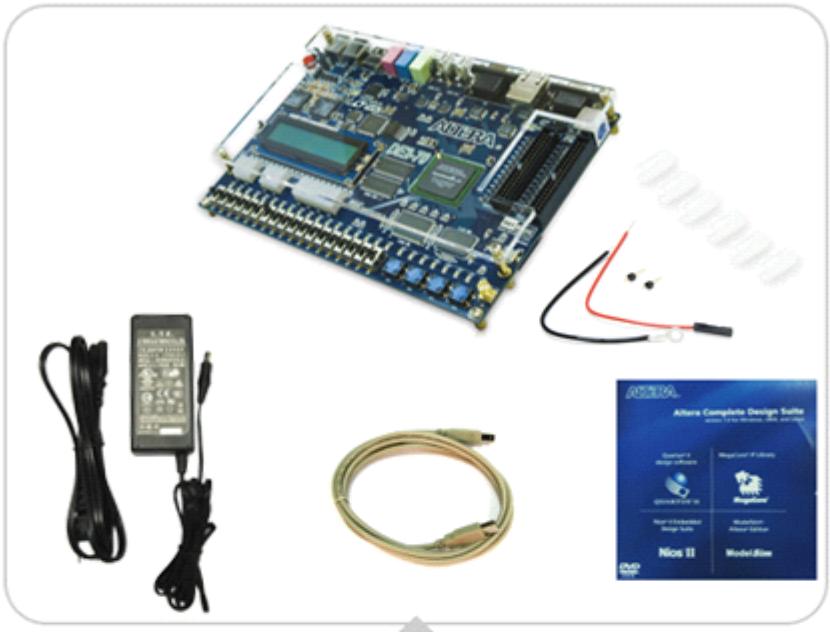
DE2-70 Video Utility

全球使用者实例

- 国外名校使用 DE2-70 之课程刚站
- 国外使用 DE2 之实例展示

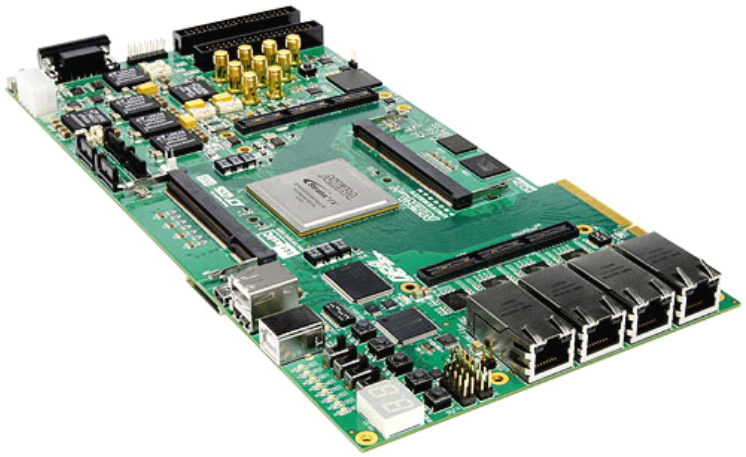
» MORE

包装内容：



- Altera DE2-70板
- 一片 DE2-70 系统相关 CD
- Altera Quartus II DVD with Nios II - Version 7.2 (我们免费提供的软件会有使用上的一些限制，详情请参考 ALTERA 网站)
- 变压器 Adapter DC 12V/2A (美规插头)
- 1 条 USB Cable
- 6 个硅胶脚套
- 2 条 cable 线(一红一黑)
- 2 个单脚排针

Altera DE4 Development and Education Board



The DE4 Development Board provides the ideal hardware platform for system designs that demand high-performance, serial connectivity, and advanced memory interfacing. Developed specifically to address the rapidly evolving requirements in many end markets for greater bandwidth, improved jitter performance, and lower power consumption. The DE4 is powered by the Stratix® IV GX device and supported by industry-standard peripherals, connectors and interfaces that offer a rich set of features that is suitable for a wide range of compute-intensive applications. The evaluation of transceiver performance for jitter, protocol compliance, and equalization on the DE4, exceeded the Stratix IV GX performance standard with transceivers operating at 10 Gbps on SATA and HSMC interfaces!
The advantages of the Stratix® IV GX FPGA platform with embedded transceivers has allowed the DE4 to fully compliant with version 2.0 of the PCI Express standard in addition to serial ATA (SATA) interfaces making it possible to leverage the integration option for storage applications. The DE4 delivers fully tested and supported connectivity targeted reference design that integrates built-in blocks for PCI Express, SATA transceivers, and Gigabit Ethernet protocol. Situated on the DE4 also includes two DDR2 SO-DIMM socket supporting maximum capacity of 8-Gbyte of volatile memory for user applications which are capable running at 400 MHz clock rate.
The DE4 is supported by multiple targeted reference designs and two High-Speed Mezzanine Card (HSMC) connectors that allow scaling and customization with mezzanine daughter cards. For large-scale ASIC prototype development, it can be established by a cable connecting to multiple DE4/FPGA boards through the HSMC connectors.

The board features the following major component blocks:

FPGA Devices

EP4SGX230

- 228,000 logic elements (LEs)
- 17,133K total memory Kbits
- 1,288 18x18-bit multipliers blocks
- 2 PCI Express hard IP blocks
- 744 user I/Os
- 8 phase locked loops (PLLs)

EP4SGX530

- 531,200 logic elements (LEs)
- 27,376K total memory Kbits

- 1,024 18x18-bit multipliers blocks
- 4 PCI Express hard IP Blocks
- 744 user I/Os
- 8 phase locked loops (PLLs)

FPGA Configuration

- JTAG and Fast Passive Parallel (FPP) configuration
- On-board USB Blaster

Memory Devices

- 64 MB Flash with a 16-bit data bus
- 2 MB ZBT SSRAM
- I2C EEPROM

Two DDR2 SO-DIMM Sockets

- 400 MHz clock rate
- Maximum theoretical bandwidth of over 102 Gbps
- Up to 8-Gbyte capacity in total

SD Card Socket

- Provides SPI and 4-bit SD mode for SD Card access

Buttons, Switches and LEDs

- 4 push-buttons
- 4 slide switches
- 8 LEDs
- 8-position DIP switch

Two Seven Segments

- Two independent seven segments

On-Board Clocks

- 3 Programmable PLLs configured via FPGA
- o HSMA, HSMB transceiver clock source
- o SATA reference clock
- o FPGA LVDS clock input
- 50MHz/100MHz oscillator

SMA Connectors

- 2 SMA connector for external transceiver clock input
- 4 SMA connector for LVDS clock input/output
- 2 SMA connectors for clock output
- 1 SMA connector for external clock input

Four Serial ATA Ports

- Support SATA 3.0 standard 6Gbps signaling rate
- Two host and two device ports

Four Gigabit Ethernet Ports

- Integrated 1.25 GHz SERDES

PCI Express x8 Edge Connector

- Support connection speed of Gen1 at 2.5Gbps/lane to Gen2 at 5.0Gbps/lane
- Connection established with PC motherboard with x8 or x16 PCI Express slot

Two 172-pins High Speed Mezzanine Card (HSMC)

- 2 female-HSMC connectors
- I/O voltage 2.5V
- Total of 12 high-speed transceivers at 8.5 Gbps
- Total of 38 LVDS pair at 1.6 Gbps

Two 40-pin Expansion Headers

- 72 FPGA I/O pins, as well as 4 power and ground lines, are brought out to two 40-pin expansion connectors
- 40-pin header is designed to accept a standard 40-pin ribbon cable used for IDE hard drives
- I/O voltage 3.0V

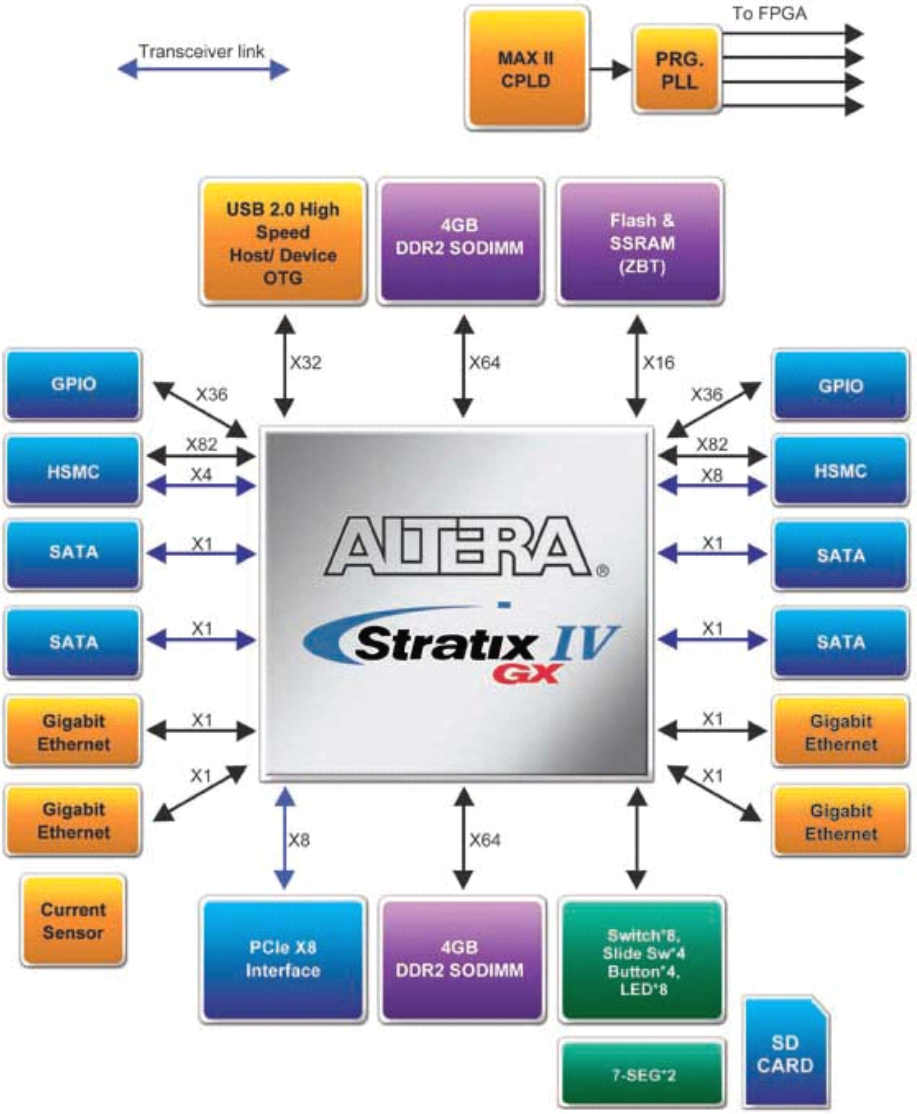
USB Host/Slave Controller

- Complies fully with Universal Serial Bus Specification Rev. 2.0
- Support data transfer at high-speed, full-speed, and low-speed
- Support both USB host and device
- Three USB ports (one type mini-AB for host/device and two type A for host)
- Support Programmed I/O (PIO) and Direct Memory Access (DMA)

Power

- DC input 12V and 3.3V
- PCI Express edge connector power
- Support PCI Express external standard power source
- On-Board power measurement circuitry

Block Diagram



- Size：142.46*278.64 mm

Download

DE4 Control Panel

DE4 System Builder

Document

Title

Version

Size(KB)

Date Added

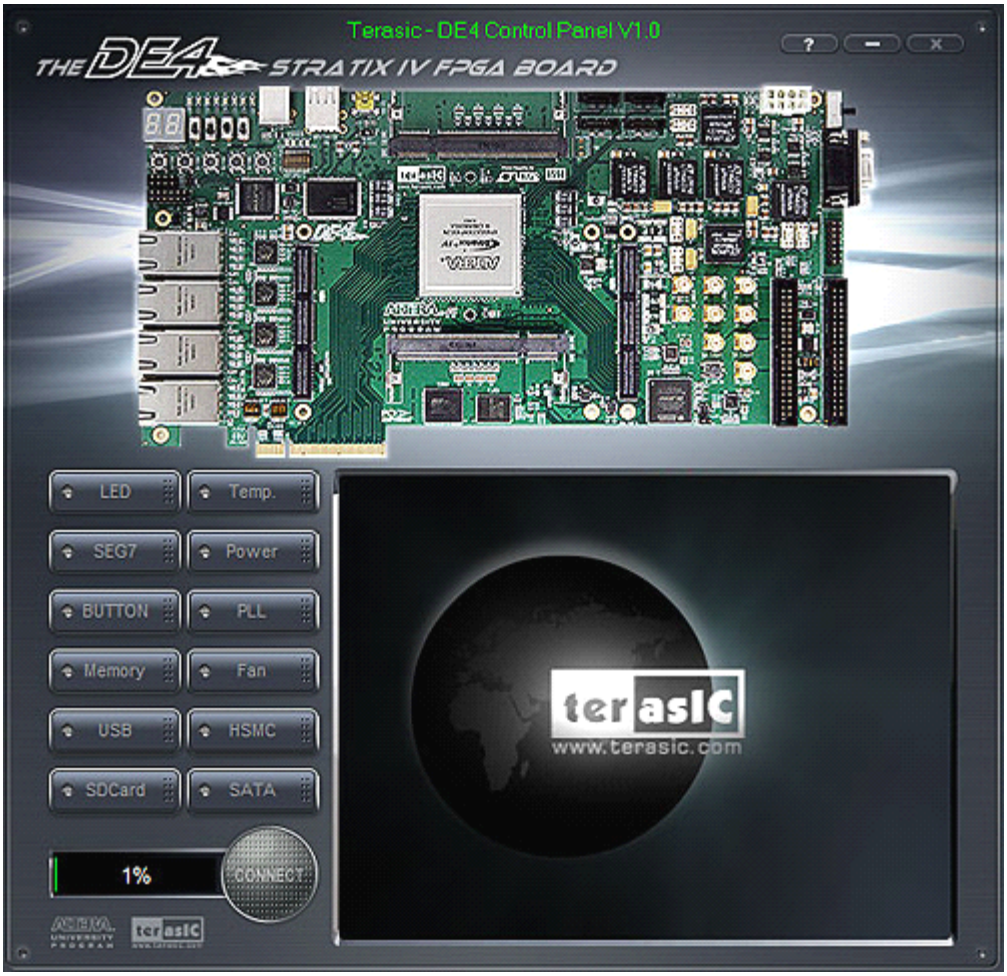
Download

DE4 User manual - - - -

DE4 Tools

DE4 Control Panel - allows users to access various components on the DE4 board from a host computer.

DE4 Control Panel



DE4 System Builder - a powerful tool comes with the DE4 board. This tool will allow users to create a Quartus II project file on their custom design for the DE4 board. The top-level design file, pin assignments, and I/O standard settings for the DE4 board will be generated automatically by the DE4 System Builder. In addition, through the HSMC connectors you can select various daughter

cards in conjunction with the DE4 using the DE4 System Builder.

DE4 System Builder

The generated Quartus II project files include the following:

- Quartus II Project File (.qpf)
- Quartus II Setting File (.qsf)
- Top-Level Design File (.v)
- External PLL Contorller (.v)
- Synopsis Design Constraints file (.sdc)
- Pin Assignment Document (.htm)

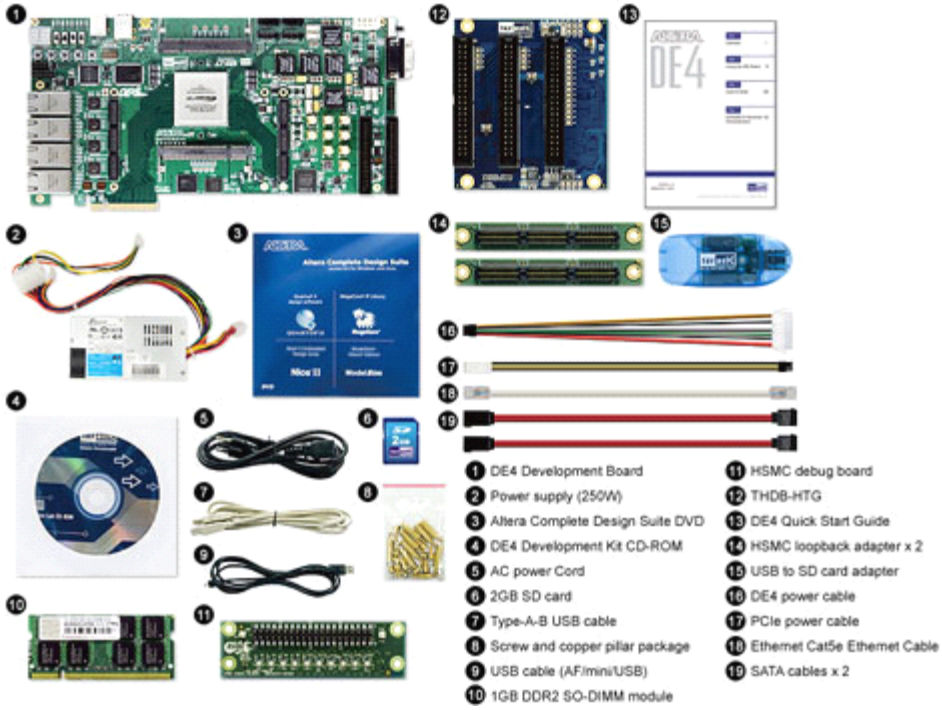
DE4 Demonstrations

Reference Designs

- USB Host/Device
- Ethernet - Simple Socket Server

- PCIe Simple I/O Control
- Power Measurement
- SATA Loopback
- HSMC Loopback
- SD Card reader
- PLL IP Configuration
- DDR2 SDRAM

The DE4 package includes:



4.3 英寸数字 LCD 触碰面板套件

The 4.3″ Ultra-high Resolution LCD Touch Panel Development Kit provides users a 800x480 full-color high-quality LCD Touch Panel with complete reference designs and source code allowing users to develop applications by a touch panel on the Altera DE3/DE2-70/DE2/DE1/DE0 board and Altera Cyclone II Starter Kit.

最新推出 4.3 英吋数字 LCD 触碰面板套件 - 附有触碰式数字像框及图像产生器等参考设计与所有原始程序代码(Verilog)

- 完整触碰式数字像框及图像产生器等参考设计与所有原始程序代码
- 4.3 英吋数字 LCD 触碰面板操作手册
- 与 Altera DE2-70/DE2/DE1/Cyclone II Starter board 之联机
- Size：127*87 mm

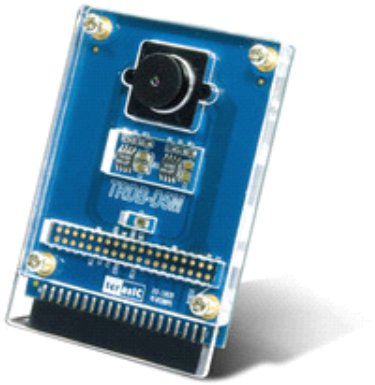
提供触碰式数字像框及图像产生器等参考设计原始程序代码

本套件适用于 Altera DE3/DE2-70/DE2/DE1/DE0/Cyclone II Starter Boards

包装内容：

- One 4.3″ LCD Touch Panel Package
- One System CD

500 万像素数字相机模块卡



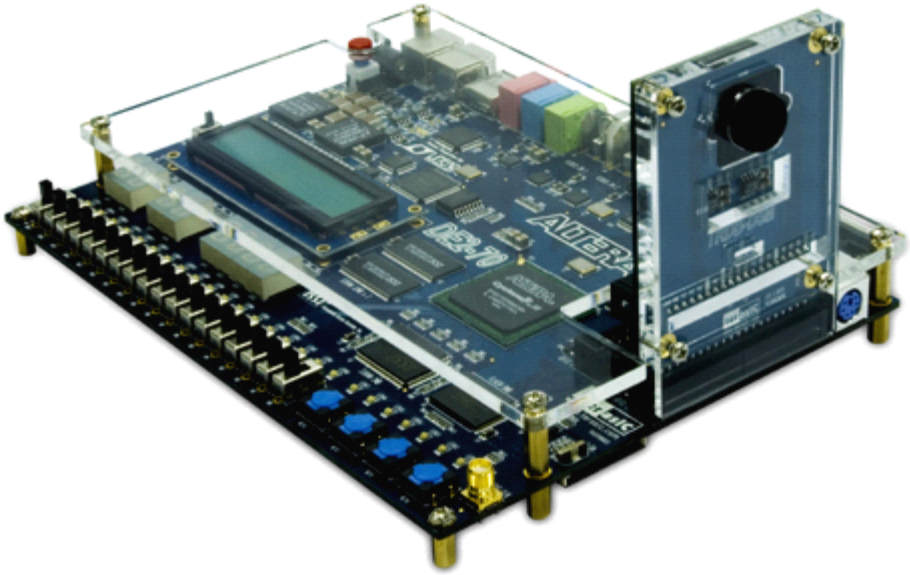
本套数字相机模块卡提供使用者在友晶科技 FPGA 平台上开发五百万画素相机所需要的所有相关信息，内容包括了使用 Verilog 语言所发展的硬件设计，以及将相机模块所拍画面转成 BMP/JPG 文件然后上传到 PC 的软件工具程序。本份初次使用者说明手册将引导，导致使用者如何来练习使用数字相机模的各种功能。

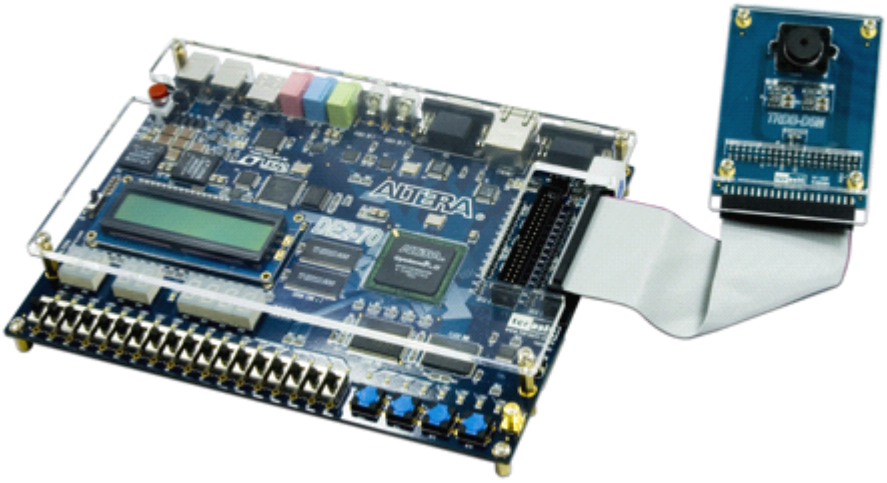
500万像素数字相机套件

- Complete reference design with source code in Verilog
- A User Manual with Live Demo examples
- Support exposure time controlling - users can adjust the exposure according to the light of the surrounding area
- Support motion capture mode
- Software allows users to upload the picture captured into PC and save the picture into bitmap format or Joint Photographic Experts Group for viewing.
- Equipped with Micron 5 Mega Pixel CMOS sensor
    - Support 2,592H x 1,944V active pixels
    - Output data in RGB Bayer Pattern format
    - Full resolution frame rate up to 15 frame per second(FPS)
- Provide users entire reference design (Frame Grabber, high-performance multi-port SDRAM frame buffer, image processing IPs)
- Support Altera DE3/ DE2_70/ DE2/ DE1/DE0 and Cyclone II Starter boards
- Size: 78*59.5 mm

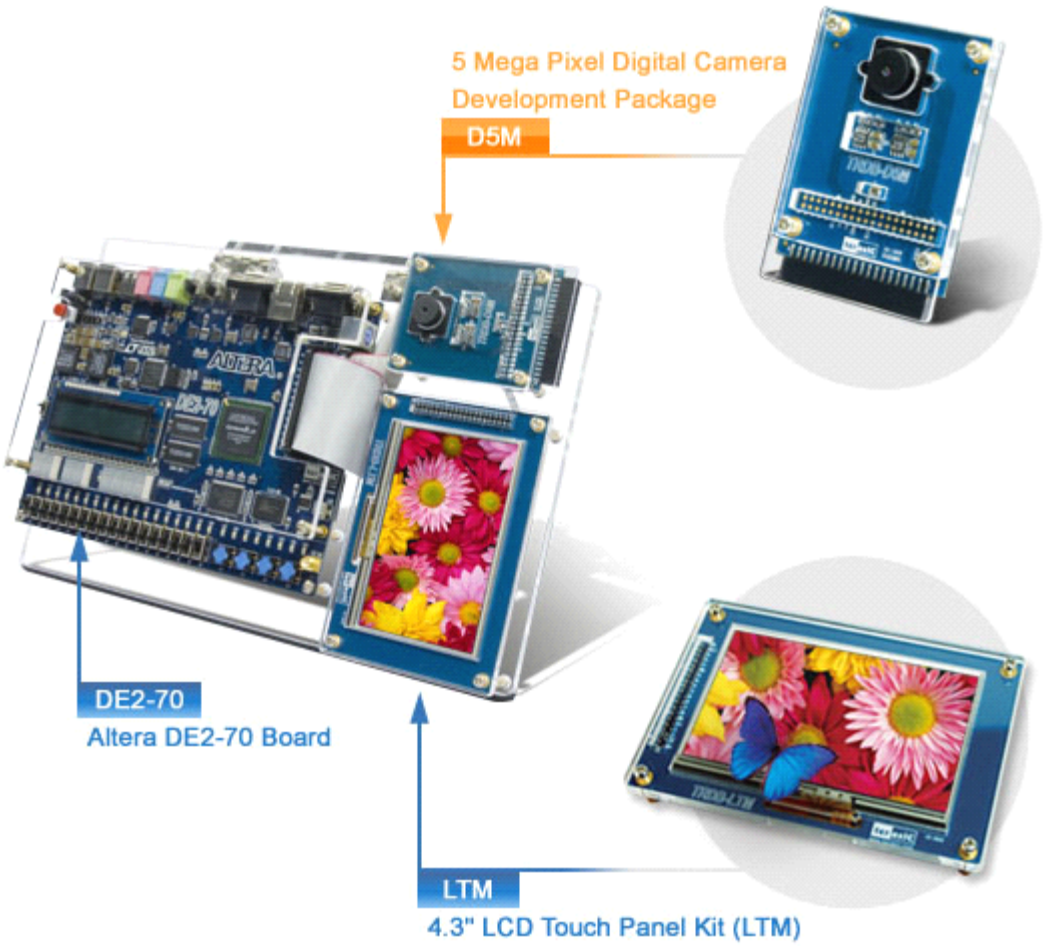
連接性

TRDB_D5M 模块是设计用来搭配 Altera DE3 / DE2 / DE2-70 / DE1 /DE0 以及 Cyclone II Starter board 使用





除了使用 VGA 屏幕之外，使用者可以选购友晶科技所设计的 4.3″ LCD 控制面板模块（ TRDB_LTM ）来当做五百万画素数字相机所拍摄画面的显示装置。

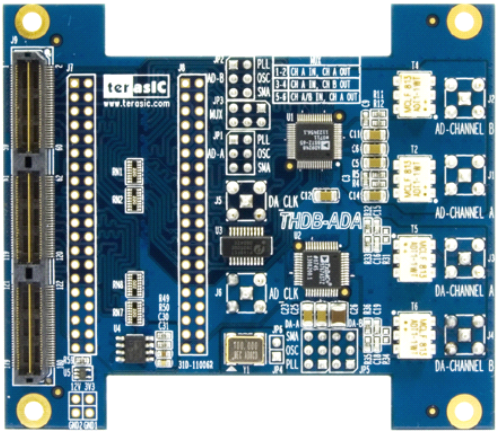


档案下载

D5M 数字相机发展套件的内容包括了下列几项

- TRDB-D5M 相机模块
- 友晶科技 D5M 光盘

ADA-HSMC 高速 数位-模拟/模拟-数位 模组卡-HSMC



ADA-GPIO

- 双倍通道
- 双倍威力
- 轻巧的板卡设计

THDB_ADA 子板為 DE 系列、Cyclone III Starter Kit 及其他有 HSMC 或 GPIO 介面的 FPGA 平台提供了 DSP 的解决方案。

AD/DA 子板

功能介绍

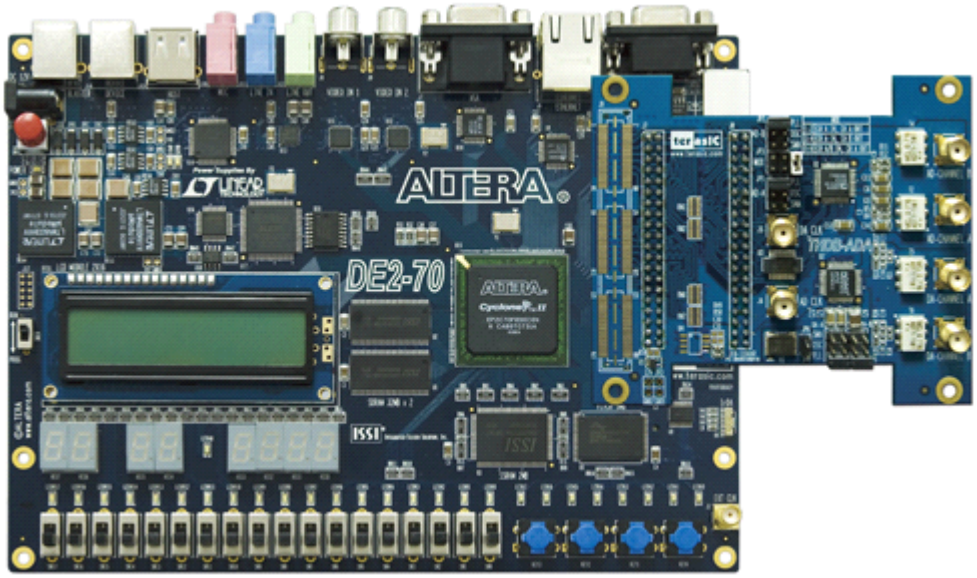
- 双 AD 通道提供14位分辨率和高达65 MSPS 的传输速率
- 双 DA 通道提供，14位分辨率和高达125 MSPS 的传输速率
- 提供 HSMC 和 GPIO 双接口,可兼容于 Cyclone III 入门套件或 DE0/DE1/DE2/DE3 开发套件系列
- 时脉来源可以来自100MHz 振荡器 、AD/DA 通道的 SMA 接口、HSMC/GPIO 接口上的 PLL 界面
- 尺寸：90.3*78.2毫米

应用特色

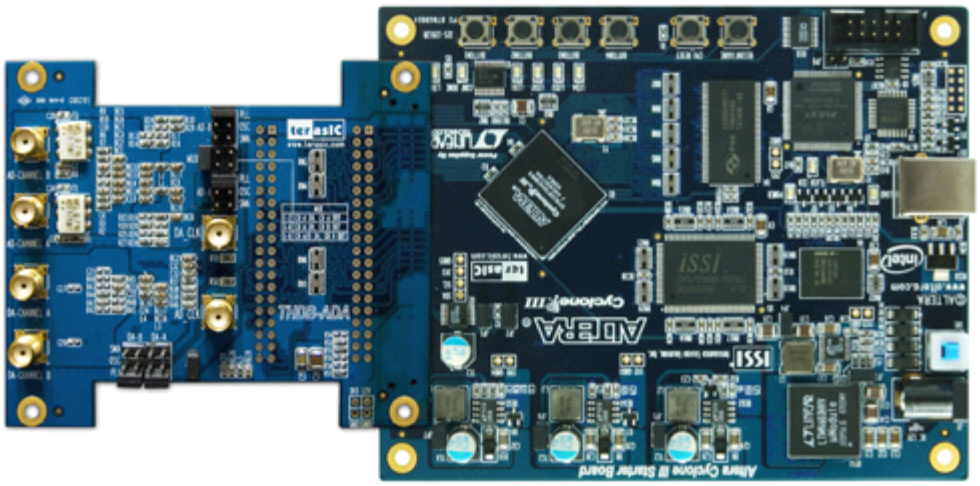
- 低成本示波器及讯号产生器
- 通讯收发器
- 数位讯号处理
- Platform for various modulation techniques

连接性

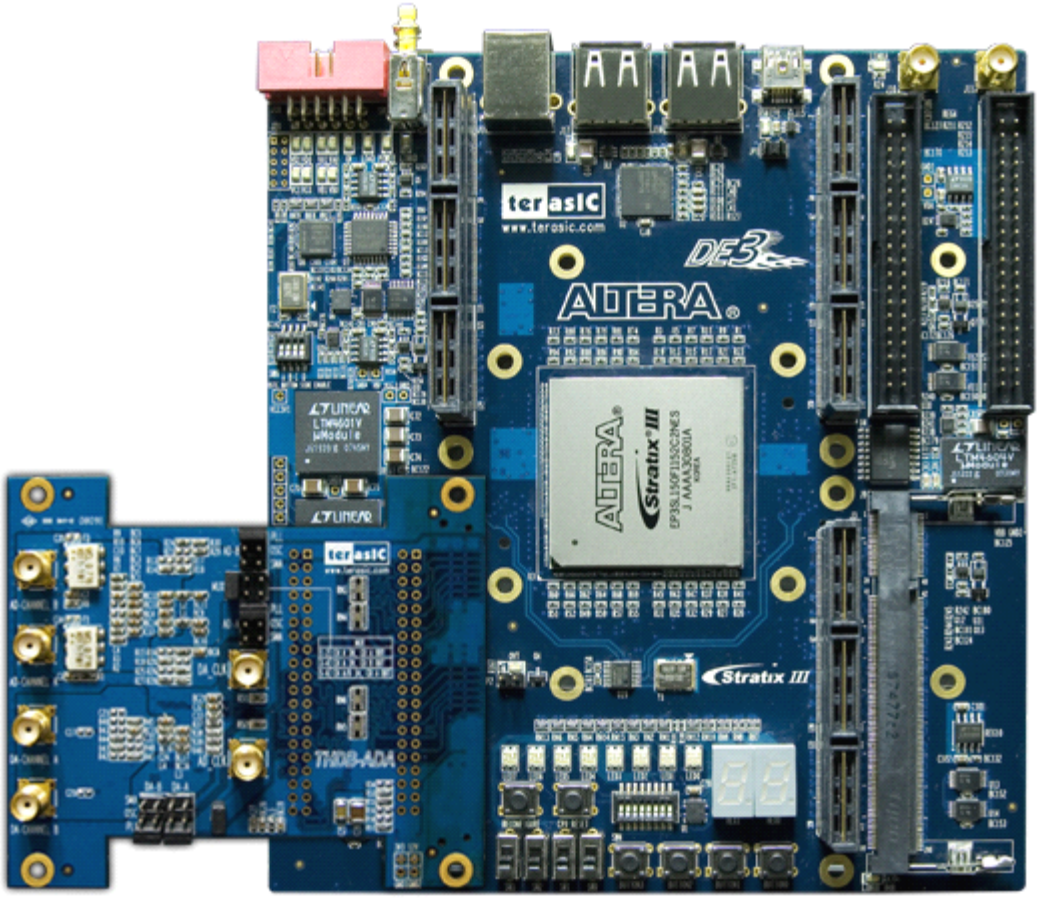
THDB_ADA 共有 ADA-GPOP 及 ADA-HSMC 两种模组来与 DE3 / DE2_70 / DE2 /DE1 及 Cyclone III Starter Kit 等开发板连接在一起。



ADA-GPIO 与 DE2-70 连接示意图



ADA-HSMC 与 Cyclone III Starter Kit 连接示意图



ADA-HSMC 与 DE3 连接示意图

参考设计

- 任意波形产生器

DE3 上任意波形产生器之结构图

- 快速傅利叶转换 (Fast-Fourier Transform) 分析

14-bit DAC B 输入资料的归一化频谱图 (Normalized Spectral Plot)

14-bit ADC B 输入资料的归一化频谱图 (Normalized Spectral Plot)

包装内容：

- One AD/DA Board
- One System CD